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EXAMINER	
JACOB, MARY C	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/603,055	BLASI ET AL.	
	Examiner	Art Unit	
	Mary C. Jacob	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-8 and 10-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-8 and 10-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The response filed 6/29/07 has been received and considered. Claims 1,3-8, 10-28 are presented for examination.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/29/07 has been entered.

Drawings

3. The objections to the drawings recited in the Office Action dated 2/23/07 have been withdrawn in view of the amendments to the specification, filed 6/29/07.

Specification

4. The abstract of the disclosure is objected to because line 10 recites the term "said". Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1, 3-8, 10-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claims 1 and 8 recite limitations that include "selecting" "suitable types of tests" based on a match between the entered configuration data of the memory model under test and the catalogued memory models from the repository. It is unclear how these tests are "selected" and where they are selected from. There is no previous limitation reciting a list of tests stored somewhere.

8. Claims 3 and 10 recite the limitation "said Hardware Description Language" in line 2. There is insufficient antecedent basis for this limitation in the claim.

9. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: the verifying of the memory model under test. The claim is directed to "a method for verifying integrated circuits specified by integrated circuit memory models", however, the claim concludes with the generation of test benches for a memory model under test, and fails to recite a step where the memory model under test is actually "verified".

10. Claim 8, line 13 recites, "setting-up by executing". It is unclear what is being "set up". For example, are the "test benches" "set up"?

11. Claims 15 and 22 recite, "compare the specific integrated circuit model to characteristic data in the repository to identify tests applicable to that specific integrated circuit model". It is unclear how comparing the circuit model to the characteristic data "identifies tests" since there are no "tests" recited in any previous limitations of the claims that could be identified. Are the tests stored somewhere?

12. Claims 15 and 22 recite, "executing a software-based test case file generation algorithm which generates specific test vectors for each of the identified applicable tests that are unique to the configured integrated circuit model in accordance with received model data". It is unclear whether "specific test vectors" are "generated" "in "accordance with received model data". For example, is the received model data used to generate these test vectors? Or, is "the configured integrated circuit model in accordance with received model data" again reciting that the "configured integrated circuit" is "configured" with the received model data, as is set forth in the limitation wherein the model data is processed in view of the identified specific integrated circuit model to produce a configured integrated circuit model suitable for simulation?

13. Claims 19 and 26 first recite, "the integrated circuit models in the repository", however, Claims 15 and 22 only recite that the "repository" stores "functional and structural characteristic data *for integrated circuit models*", leading to the interpretation that the claimed repository does not store actual integrated circuit models. Therefore, it is unclear whether the repository stores integrated circuit models or not. Claims 19 and 26 also recite, "the received specific integrated circuit model to be tested", however, Claims 15 and 22 recite receiving an "*identification* of a specific integrated circuit model

to be tested", leading to one possible interpretation that the processing functionality receives a name of a specific model to be tested and does not receive and actual model to be tested. Therefore, it is unclear whether the processing functionality receives an "identification" of a model to be tested, or an actual "model", such as a description in a hardware description language.

14. Claim 22 recites the limitation "the repository" in line 8. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

17. Claims 1, 3, 6-8, 10, 13-16, 19, 21-23, 26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zarrineh et al ("Automatic Generation and Validation of Memory Test Models for High Performance Microprocessors", Proceedings of the 2001 International Conference on Computer Design, pages 526-529, 23-26 Sept, 2001) in view of Kebichi et al (US Patent 6,671,843).

18. As to Claims 1 and 8, Zarrineh et al teaches: a computer based test bench generator for verifying an integrated circuit memory model, comprising: a repository storing an identification of memory models catalogued according to memory type, number of ports and synchronous/asynchronous functional operation (Section 3.1: paragraph 1, sentence 1, paragraph 2, and paragraphs 3-5, descriptions of RAM, CAM and FIFO primitives; section 3.3, sentence 2); means for entering behavior data of a memory model under test, the behavior data comprising an identification of ports in the memory model under test and a description for each such port of port cycles and port behavior (section 3.2, sentences 1 and 2; section 3.3, sentences 4-5); means for entering configuration data of the memory model under test (section 3.2, sentences 1 and 2); means for automatically generating test benches, said means being configured to generate tests based on a match between the entered configuration data of the memory model under test and the catalogued memory models from said repository (section 3.3; section 4.1, paragraph 1, sentence 1 and paragraph 2, sentences 3-7) and further setup by executing a software-based test case file generation algorithm which generates specific test vectors that are unique to the memory model under test

according to the configuration and behavior data (section 4.1, paragraph 2, sentences 3-8).

19. As to Claims 15 and 22, Zarrineh et al teaches: a test bench generator for integrated circuit designs, comprising: a repository which stores functional and structural characteristic data for integrated circuit models (Section 3.1: paragraph 1, sentence 1, paragraph 2, and paragraphs 3-5, descriptions of RAM, CAM and FIFO primitives; section 3.3, sentence 2); a processing functionality which receives and identification of a specific integrated circuit model to be tested along with model data describing the configuration and behavior of that specific integrated circuit model (section 3.2, sentences 1 and 2), the processing functionality operating to: process the model data in view of the identified specific integrated circuit model to produce a configured integrated circuit model suitable for simulation (section 3.3, sentences 2-5); and execute a software-based test case file generation algorithm which generates specific test vectors that are unique to the configured integrated circuit model in accordance with received model data (section 4.1, paragraph 1, sentences 3-7).

20. Zarrineh et al does not expressly teach: (claims 1, 8) selecting suitable types of tests for verifying the integrated circuit memory model and generating specific test vectors for each of the selected test types; (claims 15, 22) comparing the specific integrated circuit model to characteristic data in the repository to identify tests applicable to that specific integrated circuit model.

21. Kebichi et al teaches a method that provides a user with the ability to define its own built-in-self-test (BIST) controller test algorithms for memory (column 1, lines 52-

54) since the standard test algorithms for use in a BIST controller to test embedded memories are general in nature and not optimal for a user's novel or proprietary memory design (column 1, lines 27-28 and 44-48), wherein the method includes reading a memory model from a repository (column 1, lines 63-64; column 4, lines 18-20), and identifying and selecting suitable types of tests for verifying the memory corresponding to the selected memory model (column 4, lines 1-5 and 13-33), wherein the tests include standard tests and user defined tests that generate specific test vectors for teach type of test and implementing these tests within an HDL description for the BIST controller that will test the memory corresponding to the selected memory model (column 1, line 66-column 2, line 2; column 4, lines 20-34).

22. Zarrineh et al and Kebichi et al are analogous art since they are both directed to the testing of memory designs.

23. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the computer based test bench generator for verifying an integrated circuit memory model as taught in Zarrineh et al to identify and select suitable types of tests for and generating specific test vectors for each of the selected test types for a specific integrated circuit model or memory model as taught in Kebichi et al since Kebichi et al teaches a method that allows a user to define their own built-in-self-test controller test algorithms for memory (column 1, lines 52-54) because the standard test algorithms for use in a BIST controller to test memory are general in nature and not optimal for a user's novel or proprietary memory design (column 1, lines 44-48).

24. As to Claims 3 and 10, Zarrineh et al in view of Kebichi et al teach: wherein said test benches are specified in a Hardware Description Language (Zarrineh et al: section 3.2, sentence 1; section 3.3, sentence 2-3; section 4.1, paragraph 2, sentence 4; Kebichi et al: column 2, line 66-column 2, line 2; column 4, lines 31-34).

25. As to Claims 6 and 13, Zarrineh et al in view of Kebichi et al teach: wherein said configuration data in input to said means for generating through a command line (Zarrineh et al: section 3.2, sentence 3; Kebichi et al: column 4, lines 13-22).

26. As to Claims 7 and 14, Zarrineh et al in view of Kebichi et al teach: wherein said selection of tests is based on conditional statements (Kebichi et al: column 4, lines 16-31).

27. As to Claims 16 and 23, Zarrineh et al in view of Kebichi et al teach: wherein the specific test vectors comprise a set of self-checking test benches for the specific integrated circuit model (Zarrineh et al: section 4.1, paragraph 2, sentences 3-10; Kebichi et al: column 1, lines 27-28 and lines 32-38; column 4, lines 1-5).

28. As to Claims 19 and 26, Zarrineh et al in view of Kebichi et al teach: wherein the integrated circuit models in the repository, as well as the received specific integrated circuit model to be tested are specified using a hardware description language (Zarrineh et al: section 3.2, sentence 1; section 3.3, sentence 2-3; section 4.1, paragraph 2, sentence 4; Kebichi et al: column 2, line 63-column 2, line 2; column 4, lines 31-34).

29. As to Claims 21 and 28, Zarrineh et al in view of Kebichi et al teach: a simulator functionality which applies the identified applicable tests against the configured integrated circuit model (Zarrineh et al: section 4.1, paragraph 2, sentences 3-8).

30. Claims 4, 11, 17, 20, 24 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zarrineh et al in view of Kebichi et al as applied to claims 1 and 8 above, and further in view of Allard (US Patent 7,024,346).

31. Zarrineh et al in view of Kebichi et al teach (claims 4, 11) a computer based test bench generator wherein said test benches are specified in a Hardware Description Language; (claims 17, 24) specific test vectors comprising a set of self-checking test benches for the specific integrated circuit model; and (claims 20 and 27) integrated circuit models in the repository and received specific integrated circuit model to be tested are specified in a hardware description language.

32. Zarrineh et al in view of Kebichi et al do not expressly teach (claims 4, 11, 20 and 27) wherein said Hardware Description Language is Verilog; (claims 17, 24) wherein the self-checking test benches are Verilog test benches.

33. Allard teaches that Verilog is a hardware description language that is used to design electronic systems at the system, board and component levels and is an IEEE standard that is a de facto standard for proprietary HDL's (column 1, lines 31-37), that it is known in the art to include built-in-self-test (BIST) blocks comprising synthesizable Verilog code to test embedded analog cores (column 2, lines 13-17), and further teaches an improved apparatus and method for generating test benches (column 3, lines 5-7) wherein the test bench no longer needs to be written by hand and allows for the reuse of an existing test program therein greatly reduces the time and effort needed

to write a new test program (column 3, line 66-column 4, line 4), wherein the test benches are generated in Verilog (column 5, lines 51-52).

34. Zarrineh et al in view of Kebichi et al and Allard are analogous art since they are all directed to the generation of test benches wherein the test benches are specified in a Hardware Description Language.

35. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the test bench generated in a Hardware Description Language, the self-checking test benches and the integrated circuit models specified in a Hardware Description Language as taught in Zarrineh et al in view of Kebichi et al to include wherein the test bench or self-checking test benches are generated in a Hardware Description Language such as Verilog as taught in Allard and to specify the memory models in a hardware description language such as Verilog since Allard teaches that Verilog is a hardware description language that is used to design electronic systems at the system, board and component levels and is an IEEE standard that is a de facto standard for proprietary HDL's, that it is known in the art to include built-in-self-test blocks comprising synthesizable Verilog code to test embedded analog cores, and further teaches an improved apparatus and method for generating test benches wherein the test bench no longer needs to be written by hand and allows for the reuse of an existing test program therein greatly reduces the time and effort needed to write a new test program.

36. Claims 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zarrineh et al in view of Kebichi et al as applied to claims 1 and 8 above, and further in view of Bollano et al ("The Virtual Intellectual Property Library: From Paradigm to Product", Proc. Of IP99 Conference, Santa Clara, March 1999).

37. Zarrineh et al in view of Kebichi et al teach a computer based test bench generator for verifying an integrated circuit memory model wherein the behavior data of a memory model under test is entered.

38. Zarrineh et al in view of Kebichi et al do not expressly teach the behavior data is specified in a proprietary language.

39. Bollano et al teaches a system that implements a soft IP library in the design flow to shorten the design time and lower design cost by making system know-how available as customizable, reliable and reusable design blocks through the use of a Virtual Intellectual Properties library that is composed of system level modules written in VHDL (page 1, column 1), wherein the library includes memory models wherein the behavior data of the memory models is specified in proprietary language (page 3, "Memory Model Library and Packages", paragraphs 1-2; Figure 4, "memories" library; page 4, column 2, bullets 1 and 2).

40. Zarrineh et al in view of Kebichi et al and Bollano et al are analogous art since they are all directed to the simulation of a design for an integrated circuit that includes a repository storing structural and functional behavior for a model under test and includes the input of behavioral data for a design under test.

41. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the computer based test bench generator for verifying an integrated circuit memory model wherein the behavior data of the memory model under test is entered as taught in Zarrineh et al in view of Kebichi et al to further include wherein the behavior data input is specified in a proprietary language as taught in Bollano et al since Bollano et al teaches a system that implements a soft IP library in the design flow to shorten the design time and lower design cost by making system know-how available as customizable, reliable and reusable design blocks through the use of a Virtual Intellectual Properties library that is composed of system level modules written in VHDL (page 1, column 1).

42. Claims 18 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zarrineh et al in view of Kebichi et al as applied to claims 1 and 8 above, in further view of Killian et al (U.S. Patent 6,477,683).

43. As to Claims 18 and 25, Zarrineh et al in view of Kebichi et al teaches a test bench generator for integrated circuit designs wherein specific test vectors are generated that comprise a set of self-checking test benches for a specific integrated circuit.

44. Zarrineh et al in view of Kebichi et al does not expressly teach wherein the self-checking test benches include self-checking models incorporating complex constructs for comparing data, waiting for internal events, and timing constraint checking with respect to the specific integrated circuit model.

45. Killian et al teaches a method that automatically configures a processor by generating both a description of a hardware implementation of the processor in HDL and a set of development tools such as a compiler, assembler, debugger and simulator for programming the processor from the same configuration specification (column 6, lines 32-60), which allows for a complete flow for configuration of processor hardware and software including feedback from hardware design results and software performance to aid selection of optimal configuration for the design instead of hardware and software configuration alone (column 8, lines 54-61). The method taught by Killian et al includes a test bench for integrated circuit designs that incorporates complex constructs for comparing data (column 33, lines 25-27), waiting for internal events (column 33, lines 56-59; column 34, lines 61-62), and timing constraint checking with respect to the specific integrated circuit model (column 23, lines 14-17, lines 34-40, and lines 48-52).

46. Zarrineh et al in view of Kebichi et al and Killian et al are analogous art because they are both directed to the design and verification of integrated circuit designs described in HDL using a test bench.

47. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the test benches as taught in Zarrineh et al in view of Kebichi et al to include constructs for comparing data, waiting for internal events and checking timing constraints as taught by Killian et al since Killian et al teaches a method that allows for a complete flow for configuration of processor hardware and software including feedback from hardware design results and software performance to aid

selection of optimal configuration for the design instead of hardware and software configuration alone (column 8, lines 54-61).

Response to Arguments

48. Applicant's arguments with respect to Claims 1, 3, 6-8, 10, 15, 16, 19, 21, 22, 23, 26 and 28 have been considered but are moot in view of the new ground(s) of rejection. The claims filed 6/29/07 have been amended, and newfound prior art has been applied in accordance with the amended claim language.

Conclusion

49. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

50. Devins et al (US Patent 6,658,633) teaches verifying the design of an integrated circuit chip comprised of one or more cores wherein a project core catalog comprises driver and application description files for each core, creating a system definition file for the integrated circuit chip, inputting the driver and application files along with the system definition file into a code generator and outputting a test operating system code to apply to a software simulation of the designed integrated circuit chip.

51. Le (US Patent 6,353,904) teaches a method of automatically generating a test program that allows a user to extract re-usable test data from pre-existing test programs and store the extracted re-usable test data in a template library as a test-block template,

then the user provides the names of interested cells and corresponding pin designations to extract re-usable test data from pre-existing test programs.

52. Ravindranath et al (US Patent 5,369,604) teaches a method of generating a test plan for a circuit designated with blocks of analog, digital or mixed signal components that includes selecting tests to be performed on the blocks that designated certain inputs that are to be set with predetermined test values and certain outputs that are to be compared to expected values.

53. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary C. Jacob whose telephone number is 571-272-6249. The examiner can normally be reached on M-F 7AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Mary C. Jacob
Examiner
AU2123

MCJ
8/29/07

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